Amendments to the Specification:

Please replace the paragraph on page 4, beginning at line 13, with the following paragraph. Deletions are indicated by strike-out font and additions are indicated by underline font.

--Figure 1 provides an illustration of a typical memory bus in the art. A microprocessor chipset 102 (the host) utilizes one or more memory modules 104, e.g. Dual In-line Memory Modules (DIMM). The host 102 typically communicates with the memory modules via a common memory bus. In other words, each memory module sees all address, control, and data signals being communicated on the memory bus 106. The host is able to define which memory module is intended for receipt of a message through utilization of a series of 'chip select' lines (buses) 108. In figure 1, a series of chip select 'buses' 108 is provided. In a DIMM, for example, each chip select bus 108 would provide a chip select to the front of the module and one to the backside of the module. Each chip select line 108 is associated to a specific memory module [[108]] 104. The chip select line 108 asserted provides which memory module is to receive the data currently communicated on the memory bus 106.--